REMARKS

Examiner Thomas L. Dickey is thanked for his examination of the subject Patent Application. The Specification, Drawings and Claims have been carefully reviewed with respect to the cited prior art and the Claims have been amended and are considered to be in condition for Allowance.

Claim Status

Claims 1-3, 5 and 6 remain in this application.

DETAILED ACTION

Action Item 1
Amendment Filed

1. The amendment filed on 05/12/03 has been entered.

Action Item 2
Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 05/12/03, have been approved.

Action Item 3
Claim Rejections - 35 USC §102

Reconsideration of the rejection of Claim 1 under 35 U,S,C. 102(a) as being anticipated by CHOI et al. (5,859,454) is requested based on the following reasons.

The Examiner writes:

> Choi et al. discloses a stacked-gate flash memory cell comprising a " semiconductor substrate 40 having an active area (seen directly below floating Poly-Si gate 21), a floating Poly-Si gate 21 with a bottom surface and a multiply connected top surface, the bottom surface being flat and overlying the active area, the multiply connected top surface overlying the bottom surface; the multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of the multiply connected top surface overlying the active area is greater than the area of the bottom surface, wherein the individual cross-sectional shapes are selected from a group consisting of

> rectangular, trapezoidal and triangular shapes (in this case, rectangular), a conformal inter-poly dielectric layer 42 replicating the individual cross-sectional . shapes over the floating Poly-Si gate 21; and a conformal Poly-Si control gate 33 replicating the individual cross-sectional shapes over the inter-poly dielectric layer 42. Note figure 6 of Gho! et al. Note that clain11 places limitations on g Cross-section (not, for example, all cross-sections) of a floating gate, that the floating gate 21 of Choi et al. has at least two cross-sections (two are displayed, one in figure 5 and another in figure 6) and that although the cross-section shown in figure 5 does not meet claim 1, the cross-section shown in figure 6 does in fact meet claim 1.

The Applicants intended the words "multiple regions" to include shapes beyond a single rectangle, triangle or trapezoid. Now it seems those words do not provide that limitation. Claim 1 is now amended to require more than five top surfaces that are multiply connected. With this, single rectangles, triangles and trapezoids will be precluded.

Action Item 4
Claim Rejections - 35 USC § 103

Reconsideration of the rejection of Claims 2,5, and 6 under 35 U.S.C. 103(a) as being unpatentable over CHOI et al. (5,859,454) in view of MURAI (5,243,559).

The Examiner writes:

> Choi et al. discloses a stacked-gate flash memory cell with all the limitations of claims 2,5, and 6 (including an aNa inter-poly dielectric layer 42, note column 7 lines 33-37) except certain specific dimensions for the thickness of the floating gate (190-210 nm), aNa inter-poly dielectric layer (15-25 nm), and control gate (150-200 nm) Note figure 6 of Choi et al. Choi et al. is silent on the question of what these dimensions should be. However, Murai, which was published well before Choi et al. was applied for, and would have been well known to the Choi . et al. inventors, discloses a stacked-gate flash memory cell with a floating gate 36 having a thickness in the range of 190-210 nm, an aNa inter-poly dielectric layer 37 having a thickness in the range of 15-25 nm, a.n~ a control gate 38 having a thickness in the range of 150-200 nm. Note column 4 lines 37,43, and 50 of Murai. Therefore, it would have been obvious to a person having skill in the art to build a physical realization of Choi et al.'s stacked-gate flash memory cell using the dimensions taught by Murai in order to build Choi et al.'s stacked-gate flash memory cell with a minimum of experimentation. In the absence of specific instructions from Choi et al. one having skill in the art would reasonably believe that any dimensions known to Choi et al. (such as the Murai dimensions)

would work.

Claims 2, 5 and 6 are dependent on newly amended Claim 1.

Action Item 5
Response to Arguments
None

Action Item 6
Allowable Subject Matter

6. At the suggestion of the Examiner, Claim 3 has been amended to include all the limitations of Claim 1 and Claim 3 now stands as an independent claim.

CONCLUSION

We have reviewed the related art references made of record and agree with Examiner Dickey that none of these suggest the present claimed invention.

In light of the above arguments and improved drawings, it is suggested that the Claims now clearly describes the invention. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is requested that should Examiner Dickey not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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